


Julien MASTRANGELO

French PhD student in electronics applied to nuclear instrumentation

France 

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<https://julienmas.github.io> 



EDUCATION

2022 – 2025 **PhD | CEA-list (Paris-Saclay)**

Exploration of heterogeneous high data rate streamed and programmable architectures for real time applications in nuclear instrumentation.

PhD student in Electronic Architectures, modelisation and data analysis (DRT/LIST/DIN/SIMRI/LEMA) of the CEA (French Alternative Energies and Atomic Energy Commission).

2019 – 2022 **ISMIN | Mines de St-Etienne (CGCP, Gardanne)**

Master of microelectronics and computer science engineering.

Majoring in **embedded systems**, specialisation in **mobility and security**. Analogic electronics, digital electronics, microcontroller systems. Embedded real-time computing, FPGA codesign.

2021 – 2022 **MSc Hybrid Electronics | Aix-Marseille University**

Stretchable electronics, sensors, organic optoelectronics, bioelectronics, micro-generators.

2017 – 2019 **CPGE MPSI-MP* | Lycée Pothier (Orléans)**



WORK EXPERIENCE

APR-SEP 2022 **Engineer Intern | Polytechnique Montréal (QC, Canada)**

I worked on the implementation of a **neural network** (U-Net) on a **FPGA** target, using the FINN framework.

MAR-AUG 2021 **Side-Channel Attacks Intern | Qualcomm (Cork, Ireland)**

As an engineering intern at the Qualcomm security lab in Cork, I implemented **side-channel attack** techniques in order to add features to the lab in-house tools. I led practical experimentations with continuous improvements on industrial devices by looking for new solutions in the recent scientific literature.

AUG 2019 **Digger | Departmental Archaeology Service of Aveyron**

Excavation traineeship. I worked as a volunteer on a protohistoric excavation site from the Iron Age.

2017-2020 **Summer jobs | Limpa nettoyyages (France)**

Working for Limpa, I cleaned a high school in compliance with health department regulations.



SKILLS

- **French:** native
- **English:** fluent
- **Italian:** low-intermediate
- **Coding skills:** VHDL, Codesign, embedded C, C++, Python, SQL, deep learning, web development
- **Engineering software:** Git, Vivado Design, ModelSim, STM32Cube, Proteus 8, Latex, Cisco packet tracer



INTERESTS / PROJECTS

- **VHDL modelisation and design on FPGA of the AES-128.** As a school project, I coded the four basic operations that make up the encryption of AES, the key expander function and the associated FSM. Then, I implemented this AES on an FPGA using Vivado.
- **Musician.** Trumpet, bass guitar and guitar player. I am part of the French rock band [45Tours](#) as a bass guitar player. I played an opera (Aïda from Verdi) in Orléans's Zénith.
- **Password wallet.** Password wallet is a C-coded program to save passwords based on SHA-256 hash function and XOR-encryption. Source code is available on [my GitHub](#).